WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor device comprising the steps of:

(a) forming a wiring layer on a semiconductor substrate having an integrated circuit and a pad electrically connected to the integrated circuit, the wiring layer being electrically connected to the pad;

(b) forming a resin layer covering the wiring layer;

(c) forming a first concave portion at an area of the resin layer, the area overlapping the wiring layer, by a first process;

(d) forming a through-hole in the resin layer by removing a bottom of the first concave portion by a second process, the second process differing from the first process, and forming a second concave portion in the wiring layer in such a way that an angle between an osculating plane at any point of a surface of the second concave portion and a top surface of the wiring layer, with the angle being defined outside the second concave portion is 90° or more; and

(e) providing an external terminal in the second concave portion of the wiring layer.

2. The method for manufacturing the semiconductor device according to claim 1, wherein, in step (c), the first concave portion is formed in such a way that an angle between the osculating plane at any point of a surface of the first concave portion and a top surface of the resin layer, with the angle being defined outside the first concave portion is 90° or more.

3. The method for manufacturing the semiconductor device according to claim 1, wherein, in step (b), the resin layer is formed of a thermosetting resin

precursor and, prior to step (d), the thermosetting resin precursor is heated.

4. The method for manufacturing the semiconductor device according to claim 1, further comprising forming the resin layer of a resin precursor that is sensitive to radiation, and the first process includes irradiation with the radiation and development of the resin precursor.

5. The method for manufacturing the semiconductor device according to claim 1, wherein the second process comprises dry etching.

6. The method for manufacturing the semiconductor device according to claim 1, further comprising forming the resin layer of a solder resist.

7. The method for manufacturing the semiconductor device according to claim 1, further comprising providing the first concave portion with a curved outline at a cross section taken along a plane perpendicular to a top surface of the resin layer.

8. The method for manufacturing the semiconductor device according to claim 1, further comprising providing the second concave portion with a curved outline at a cross section taken along a plane perpendicular to the top surface of the wiring layer.

9. The method for manufacturing the semiconductor device according to claim 1, further comprising providing the first concave portion with a width that decreases with a depth of the first concave portion.

10. The method for manufacturing the semiconductor device according to

claim 1, further comprising providing the second concave portion with a width that decreases with a depth of the second concave portion.

11. The method for manufacturing the semiconductor device according to claim 1, further comprising forming the second concave portion in such a way that an opening thereof is entirely disposed inside the through-hole.

12. A semiconductor device comprising:

a semiconductor chip having an integrated circuit and a pad electrically connected to the integrated circuit;

a wiring layer electrically connected to the pad and having a concave portion, the concave portion being formed in such a way that an angle between an osculating plane at any point of a surface of the concave portion and a top surface of the wiring layer, with the angle being defined outside the concave portion, is 90° or more;

an external terminal joined to the concave portion of the wiring layer; and

a resin layer provided on the wiring layer, the resin layer having a through-hole, the through-hole and the concave portion overlapping each other.

13. The semiconductor device according to claim 12, wherein the concave portion has a curved outline at a cross section taken along a plane perpendicular to the top surface of the wiring layer.

14. The semiconductor device according to claim 12, wherein the concave portion has a width that decreases with a depth of the concave portion.

15. The semiconductor device according to claim 12, wherein the concave portion is formed in such a way that an opening thereof is entirely disposed

inside the through-hole.

16. The semiconductor device according to claim 12, wherein the external terminal contacts the through-hole in the resin layer.

17. The semiconductor device according to claim 12, further comprising a stress relief layer formed on or above the semiconductor chip wherein the wiring layer is formed on or above the stress relief layer.

18. The semiconductor device according to claim 12, wherein the resin layer is formed of a solder resist.

19. A circuit board including the semiconductor device according to claim 12.

20. An electronic instrument including the semiconductor device according to claim 12.

21. A semiconductor wafer comprising:

a semiconductor substrate having a plurality of integrated circuits and pads electrically connected to the plurality of integrated circuits;

a wiring layer electrically connected to the pads and having concave portions, the concave portions being formed in such a way that an angle between an osculating plane at any point of a surface of each of the concave portions and a top surface of the wiring layer, with the angle being defined outside each of the concave portions, is 90° or more;

external terminals joined to the concave portions in the wiring layer; and

a resin layer provided on the wiring layer, the resin layer having through holes, the through holes and the concave portions overlapping each other.

22. The semiconductor wafer according to claim 21, wherein each of the concave portions has a curved outline at a cross section taken along a plane perpendicular to the top surface of the wiring layer.

23. The semiconductor wafer according to claim 21, wherein each of the concave portions has a width that decreases with a depth of each of the concave portions.

24. The semiconductor wafer according to claim 21, wherein the concave portions are formed in such a way that openings thereof are entirely disposed inside the through holes.

25. The semiconductor wafer according to claim 21, wherein the external terminals contact the through holes in the resin layer.

26. The semiconductor wafer according to claim 21, further comprising a stress relief layer formed on or above the semiconductor substrate wherein the wiring layer is formed on or above the stress relief layer.

27. The semiconductor wafer according to claim 21, wherein the resin layer is formed of a solder resist.